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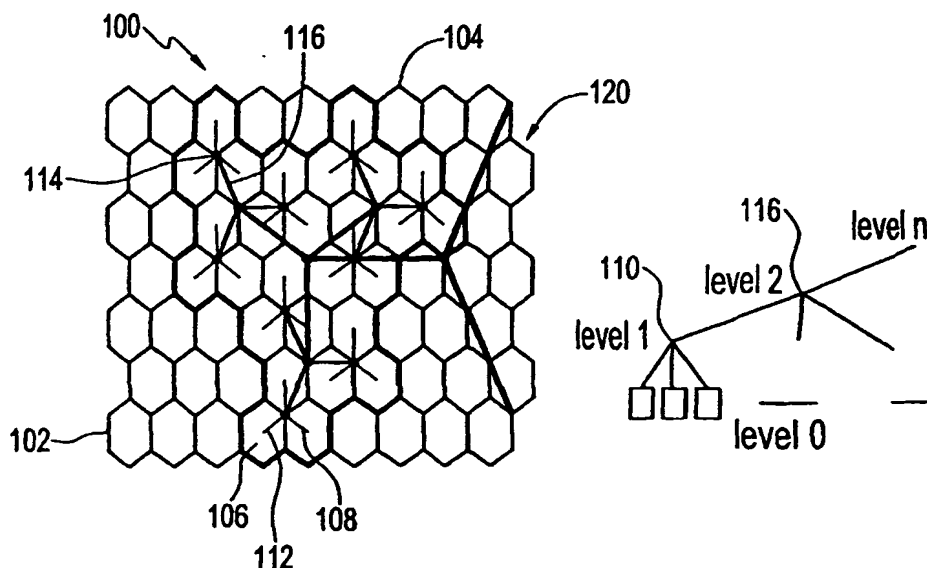
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(54) Title: INTERCONNECTION ARCHITECTURE AND METHOD OF ASSESSING INTERCONNECTION ARCHITECTURE



(57) Abstract: A multi-celled chip 100. The chip includes a plurality of hexagonal cells 104 arranged in an array 102. A plurality of interconnects including Y's 108 connect the cells in clusters 106 of three cells each, so that each of the cells is interconnected.